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(54) Programmable logic device with multi-function input pin

Programmierbare logische Schaltung mit Multifunktionseingangspin

Dispositif logique programmable avec broche d'entrée multi-fonction

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- ELECTRONIC DESIGN. vol. 37, no. 12, June 1989, HASBROUCK HEIGHTS, N pages 87 - 90; Dave Bursky: "Programmable Logic IC Tackles many Tasks"

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Description

The present invention relates generally to integrated circuit devices, and more specifically to a programmable logic device.

Programmable logic devices are becoming increasingly popular in the electronics industry because of their flexibility. These devices allow a user to configure a standard part to perform a wide variety of logic functions. Since a single standard device can be configured many different ways, the total cost of using such a device in a system can be significantly less than the cost of custom designed parts; especially in cases where product volume is not extremely large.

One popular type of programmable logic device has evolved from simpler programmable logic arrays (PLA). These devices include an AND-OR array. In such an array, a plurality of row input lines cross a plurality of product term output lines in such a manner that any row line may be connected to any or all of the product term lines. This is generally implemented as a rectangular grid of horizontal and vertical overlapping signal lines, with the capability of making a connection between two signal lines at each cross-point. The row lines all run in one direction, while the product term signal lines run at right angles to the row lines.

In general, row signal lines are provided to represent the true and inverted values for all input signals to the device. The connection of row signal lines to the product term signal lines provides the AND function of the array. Groups of product term signal lines are OR'd together to provide the OR function of the array. Each group of product term signal lines which are OR'd together are connected to an output logic block which provides output signals to an input/output pin. These output logic blocks are often referred to as output logic macrocells (OLMC).

A typical programmable logic device has several dedicated input pins, which are used solely to provide input signals to the array. Input/output pins connected to the output logic macrocells can typically be programmed to function as output pins, being driven by the associated output logic macrocells, or as additional input pins. When an input/output pin is programmed to function as an input, the associated output logic macrocell is not used. Output logic macrocells typically include both combinatorial and sequential logic, either of which can be used to drive the input/output pin when it is programmed to provide an output signal. The functions of the output logic macrocells are defined at device program time as known in the art.

Many programmable logic devices also include multi-function input pins. These pins can be used as data inputs, in which case they function the same as the dedicated input pins. Alternatively, they can be programmed to perform various control functions, and are used to provide signals such as a device clock signal (used to drive sequential circuitry), input latch enable, and output enable. As is the case with the remainder of the device, these multi-function input pins are programmed to perform a selected function at device program time, with the programming information typically being stored in EEPROM or a similar non-volatile storage. The article "Programmable logic IC tackles many tasks" by D.BURSKY in ELECTRONIC DESIGN, vol.37, no.12, 8th June 1989, Hasbrouck Heights; NJ, US, pages 87-88 and 90 shows such a multifunctional pin, for receiving either a logic input or a clock signal.

Additional inputs to the AND-OR array can be provided by feedback signals from the output logic macrocells. When the output logic macrocells are programmed to function in this manner, an output signal is generated which is applied to a row of the array. This feedback output signal may or may not be applied to the associated input/output pin. Such a programmed function for the output logic macrocell is often referred to as a buried logic function.

Physical limitations exist on the number of rows which can be provided in the array. A single row driver, which provides a true and inverted signal to the array, is typically connected to each output logic macrocell. If the cell is programmed to provide a buried output signal, such output signal is provided to this row driver. If the associated input/output pin is programmed to function as an input, it is connected to the same row driver, and the output logic macrocell is unused.

In programmable logic devices, it is always desirable, but often difficult, to make full use of the input and output pins of the device. Providing buried outputs and using input pins to provide control signals limits the number of pins which are available for use as input and output. Using input/output pins for input is also wasteful of resources, since the associated output logic macrocells are not used. It would be desirable to provide circuitry and a device design which allows as complete as possible use of all input and input/output pins on a device.

A prior art document, US-A-4742252 discloses a programmable logic device having an AND or ARRAY, a row driver buffer having an output connected to the array, a plurality of output circuit blocks and a plurality of output multiplexers. An input pin for data is connected to the input of a selector which has an output connected to the input of the row driver and has further inputs connected to a buried register and to an output of an adjacent output circuit block.

Embodiments of the present invention provide circuitry connected to input and output signal pins which allows better utilization of AND-OR array inputs in a programmable logic device.

Embodiments of the present invention provide such circuitry which allows array row drivers for multi-function input pins to be utilized when the associated input pins are used for control functions.

Embodiments of the present invention provide such circuitry which allows output logic circuitry to be used to

generate feedback signals while using an associated input/output pin for input.

According to the present invention there is provided a programmable logic device comprising an AND-OR array, a row driver buffer having an output connected to the array, and an output logic block comprising multiplexer circuitry and logic circuitry coupled to inputs of the multiplexer circuitry, said programmable logic device further comprising an input pin, a selector having an output connected to the row driver buffer, a first input connected to the input pin and a second input connected to an output of the multiplexer circuitry, the selector further comprising a program latch for storing program information determining which selector input is connected to the selector output, wherein the input pin is further connected to buffer circuitry whereby said selector connects data from said first or said second input to said row driver buffer according to said program information, and whereby said program information causes said selector to ignore the signal on said first input when said input pin supplies control signals.

Hence, in the described embodiment, multi-function input pins in a programmable logic device are connected to select circuitry which is programmed at device program time. Output signals generated by one or more output logic macrocells are also connected to such select circuitry. The select circuitry generates a signal which is used to drive a row of the array.

If an input pin is used for providing a control signal, it is not connected to the array, and the output circuitry can drive that row of the array with an output signal which it generates, or with an input signal obtained from an associated input/output pin.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a diagram of a portion of a programmable logic device according to the present invention; and

Figure 2 is a block diagram of an output logic macrocell and associated select circuitry according to the present invention.

Referring to **Figure 1**, a programmable logic device, referred to generally with reference number **10**, contains an AND-OR array **12**. As shown in **Figure 1**, row signal lines run vertically in the drawing, and product term signal lines run horizontally. For clarity of explanation, **Figure 1** illustrates only a small number of row and product term signal lines. As will be appreciated by those skilled in the art, an actual programmable logic device constructed according to the present invention will typically have a much larger number of row and product term signal lines.

Dedicated input signal pins **14, 16, 18, 20** are connected to associated row drivers **22, 24, 26, 28**, respectively. Each row driver generates a true and inverted signal corresponding to its input. These signals are connected to separate rows within the array **12**. For example, row driver **22** generates a true signal on signal line **30** and an inverted signal on line **32**. The signal lines **30, 32** are connected to row lines **34** and **36** respectively. As is known in the art, only one input signal is connected to each row signal line, and connection may be made between any given row signal line and any or all product term signal lines in the array **12**. Each of the remaining row drivers **24, 26, 28** connected to dedicated input pins **16, 18, 20** provides input to the array **12** in a similar manner.

OR gates **38, 40, 42, 44** provide a logical OR function of several product term lines. For example, gate **40** ORs together the four product term signal lines **46**. This provides the OR function of the array **12**. Although only four product term signal lines **46** are shown connected to each OR gate, a larger number is typically provided in actual devices.

The outputs of OR gates **38, 40, 42, 44** are connected to output logic macrocells (OLMC) **48, 50, 52, 54**, respectively. Each OLMC drives an output buffer **56** and provides a buffer enable signal line **58** to enable or disable the output buffers **56**. The various output buffers **56** are used to drive the input/output pins **60, 62, 64, 66** associated with the OLMCs. Input signal lines **68** are also connected to each input/output pin in order to provide a signal path between the input/output pin and the associated OLMC when such pin is used for input.

Each OLMC **48, 50, 52, 54** provides an output signal to an associated row driver **70, 72, 74, 76**. As described above, each row driver **70-76** provides true and inverted inputs to the array **12**.

Input pin **78** is a multi-function pin used to provide either an input signal to the array **12** or a clock signal for the output logic macrocells **48-54**. Signal line **80** is used to connect input pin **78** to a select circuit **82** and a buffer **84**. As will be described in more detail in connection with **Figure 2**, when pin **78** is programmed to function as an input pin, select circuit **82** connects signal line **80** with row driver **86**. When pin **78** is programmed to provide a clock signal, select circuit **82** ignores all signals present on line **80**. Instead, buffer **84** provides a clock signal on line **88** to each of the OLMCs. When pin **78** is used as an input pin, each of the OLMCs is programmed to ignore the signal which is present on clock signal line **88**. Alternatively, buffer **84** can be programmed to generate a fixed value regardless of input.

Pin **100** is also a multi-function pin. It can be programmed to provide an input signal to the array, or to provide a latch enable (LE) signal to latch the signals present on input pins **14-20**. When pin **100** is programmed to function as an input pin, signal line **102** connects input pin **100** to select circuit **104**. Select circuit

104 connects the signal on line 102 to row driver 106, which applies the signal present on input pin 100 to the array 12.

When pin 100 is programmed to function as a latch enable signal, select circuit 104 ignores all signals present on line 102. Instead, buffer 108 is used to generate a latch enable signal on line 110. Signal line 110 is connected to input latches 112, which are used to latch the current values of the signals available on input pins 14-20 when the signal on pin 100 has the appropriate value. When pin 100 is being used as an input pin, latches 112 are programmed to ignore the output of buffer 108, and the signals on input pins 14-20 are transmitted directly to the associated row drivers 22-28.

Select circuits 82, 104, in addition to being connected to signal lines 80, 102 as described above, are connected to outputs from the adjacent OLMCs. Thus, select circuit 82 has three inputs: one found on signal line 80 and one each provided by OLMCs 48 and 50. A selected one of these inputs can be connected to row driver 86, with the input to be connected being selected at device program time. If desired, select circuit 82 can be programmed to connect no inputs to row driver 86. The OLMCs can be programmed to provide one of several possible outputs directly to the associated row driver and the adjacent select circuit. This allows a wide variety of input signal combinations to be connected to the array 12. For example, if pin 78 is used to provide a clock signal, OLMC 48 can be programmed to provide a buried output feedback signal to row driver 70, and to use input/output pin 60 as an input by connecting it to row driver 86 through select circuit 82.

Referring to Figure 2, details are shown of a preferred implementation for the output logic macrocells and select circuits. Only OLMC 50 is shown in detail, but the remaining OLMCs function in the same manner.

Select circuit 82 contains a multiplexer 120 having three inputs. A program latch 122 contains the program bits used to select an input line to the multiplexer 120 to be connected to row driver 86. Since three input lines are connected to multiplexer 120, two program bits must be provided by the program latch 122. The four bit combinations provided by program latch 122 cause either one of the three inputs to be connected to row driver 86, or no input (i.e., a predefined value) to be so connected.

Output logic macrocell 50 contains combinatorial logic 124 connected to the output of OR gate 40. As known in the art, various combinatorial logic functions may be defined in the combinatorial logic block 124 through the use of program latches and multiplexers. At least one combinatorial logic output signal line 126 is provided, and is preferably connected to the input of flip-flop 128, which can be, for example, a D flip-flop as shown. Flip-flop 128 has a clock input signal connected to signal line 88 as shown in Figure 1 and has a Q output connected to signal line 130. If desired, the inverted output front flip-flop 128 may be provided and connected to other logic elements, but this is not shown in Figure 2.

The outputs from combinatorial logic circuitry 124 and flip-flop 128 are provided to multiplexers 132 and 134. Multiplexer 132 is controlled by program latch 136 and provides an output signal for connection to multiplexer 120. Multiplexer 134 is controlled by program latch 138, and provides an output signal for connection to row driver 72.

The outputs from the combinatorial logic block 124 and D flip-flop 128 are also connected to multiplexer 140 which is controlled by program latch 142. Multiplexer 140 provides the output signal which is connected to output buffer 56, and either the sequential output signal from flip-flop 128, or the non-sequential signal from combinatorial logic 124, may be selected. A buffer enable signal is provided to buffer 56 on line 58 by output buffer control circuitry 144. If a multi-function input is used to provide an output enable signal (not shown), such signal will be connected to control circuitry 144 in order to provide the buffer enable signal on line 58.

As described above, pin 62 can be defined to function as either an output pin or an input pin. If pin 62 functions as an output pin, it is driven by output buffer 56 as described above. If pin 62 is to be used for input, a program latch included with output buffer control circuitry 144 applies a buffer enable signal to line 58 which permanently disables output buffer 56. Signal line 68 is then used to connect signal pin 62 with the OLMC 50.

When pin 62 is defined to function as an input pin, it is necessary that it be connected to a row driver to the array. This is accomplished by connecting signal line 68 to both multiplexer 132 and multiplexer 134. This allows the signal on input pin 62 to be used to drive either row driver 72 or row driver 86. Signal line 68 is also connected to signal line 146, which provides an output signal from OLMC 50. Signal line 146 is connected to another OLMC (not shown), and can be connected therethrough to a row driver. Signal line 148 provides an input signal from another OLMC, which may or may not be the OLMC to which signal line 146 is connected. Signal line 148 is connected to both multiplexer 132 and multiplexer 134. Signal line 148 is connected through the other OLMC to the input/output pin associated with such other OLMC. An output line analogous to output signal line 146 from the other OLMC provides the signal connected to signal line 148 in OLMC 50.

As will be appreciated by those skilled in the art, a wide variety of signal combinations may be applied to row drivers 72 and 86. This may be done in combination with use of input pin 62 as either an input pin or an output pin. For example, signal line 80 could be connected to row driver 86 through multiplexer 120; output pin 62 could be driven by the output from combinatorial logic circuitry 124, and the input/output pin of another OLMC can be used as an input pin and connected to row driver 72 through signal line 148 and multiplexer 134. As another example, a signal on line 80 could be used as a clock signal; pin 62 could be used as an input pin and connected to row driver 72 through signal line 68 and

multiplexer 134; and a buried output signal can be generated by the output of flip-flop 128, and connected to row driver 86 through multiplexer 132 and multiplexer 120.

Although only two multi-function input pins have been described, actual devices can have four or more. Any type of control function can be treated in a manner similar to that described, as will be apparent to those skilled in the art.

Use of the selection circuitry described herein allows for increased utilization of available row drivers. It also allows an output logic macrocell to be used for buried output while its associated input/output pin is used to provide an input signal to the device. This increased utilization of the limited number of input and output pins available on a programmable logic device can allow such device to be programmed to perform logic operations which could previously only be performed on programmable logic devices having a greater number of input and output pins. Such increased utilization can contribute to an overall decreased system cost for systems containing the programmable logic device.

Claims

1. A programmable logic device comprising an AND-OR array (12), a row driver buffer (86,106) having an output connected to the array, and an output logic block (48,50,52,54) comprising multiplexer circuitry (132) and logic circuitry (124,128) coupled to inputs of the multiplexer circuitry (132), said programmable logic device further comprising an input pin (78,100), a selector (82,104) having an output connected to the row driver buffer (86,106), a first input connected to the input pin (78,100) and a second input connected to an output of the multiplexer circuitry (132), the selector (82,104) further comprising a program latch (122) for storing program information determining which selector input is connected to the selector output, wherein the input pin (78,100) is further connected to buffer circuitry (108,84) whereby said selector (82,104) connects data from said first or said second input to said row driver buffer (86,106) according to said program information, and whereby said program information causes said selector to ignore the signal on said first input when said input pin (78,100) supplies control signals.

2. The device of claim 1 wherein the output logic block (50) has an input connected to the array, an input connected to a device input/output pin (62) and an output connected to the device input/output pin (62).

3. The device of claim 2 further comprising:
a second output logic block (48) having an input connected to the array (12), an input connected to a second device input/output pin (60), an output connected to the second device input/output pin (60) and an output connected to an input of said selector (82).

4. The device of claim 1, wherein the multiplexer circuitry (132) of the output logic block has an input connected to a device input/output pin (62) and said logic circuitry comprises a combinatorial logic circuit (124) and a clocked logic device (128).

5. The device of claim 1 or 4, wherein said multiplexer circuitry (132) also has an input connected to a second device input/output pin through a second output logic block.

6. A programmable logic device according to claim 1, and further comprising:-

a plurality of dedicated device input pins (14,16,18,20) connected to said array through row buffers (22,24,26,28);
a plurality of output logic blocks (48,50,52,54) having inputs connected to said array (12) and having inputs and outputs connected to device input/output pins (60,62,64,66) corresponding therewith;
wherein the multiplexer circuitry of at least one output logic block (48,50,52,54) is for providing to said selector (82,104) a signal selected from the following: an output of a combinatorial logic circuit (124) within the output logic block, an output from a clocked device (128) within the output logic block, and a signal present on the corresponding device input/output pin (62).

7. The device of claim 6, wherein said multiplexer circuitry (132) provides the signal with the further possible selection of a signal present on a device input/output pin (60,62) corresponding to an output logic block not connected directly to said selector.

Patentansprüche

1. Programmierbares Logikbauelement mit einem UND-ODER-Array bzw. einer UND-ODER-Anordnung (12), einem Zeilen-Treiberpuffer (86, 106), der einen Ausgang aufweist, der mit dem Array bzw. der Anordnung verbunden ist, und mit einem Ausgangslogikblock (48, 50, 52, 54), der einen Multiplexerschaltungskomplex (132) und einen Logikschaltungskomplex (124, 128) aufweist, der mit Eingängen des Multiplexerschaltungskomplexes (132) verbunden ist, wobei das programmierbare Logikbauelement weiter einen Eingangsstift (78, 100), eine Auswahlschaltung (82, 104), die einen

Ausgang aufweist, der mit dem Zeilen-Treiberpuffer (86, 106) verbunden ist, einen ersten Eingang, der mit dem Eingangsstift (78, 100) verbunden ist, und einen zweiten Eingang, der mit einem Ausgang des Multiplexerschaltungskomplexes (132) verbunden ist, aufweist, wobei die Auswahleinrichtung (82, 104) weiter ein Programm-Latch (122) aufweist, um Programminformation zu speichern, die bestimmt, welcher Auswahleinrichtungseingang mit dem Auswahleinrichtungsausgang verbunden ist, wobei der Eingangsstift (78, 100) weiter mit einem Pufferschaltungskomplex (108, 84) verbunden ist, wodurch die Auswahleinrichtung (82, 104) Daten von dem ersten oder dem zweiten Eingang mit dem Zeilentreiberpuffer (86, 106) gemäß der Programminformation verbindet, und wodurch die Programminformation bewirkt, daß die Auswahleinrichtung das Signal auf dem ersten Eingang ignoriert, wenn der Eingangsstift (78, 100) Steuersignale liefert.

2. Bauelement nach Anspruch 1, bei welchem der Ausgangslogikblock (50) einen Eingang, der mit dem Array bzw. der Anordnung verbunden ist, einen Eingang, der mit einem Bauelement-Eingangs-/Ausgangsstift (62) verbunden ist, und einen Ausgang, der mit dem Bauelement-Eingangs-/Ausgangsstift (62) verbunden ist, aufweist.

3. Bauelement nach Anspruch 2, das weiter folgendes aufweist:

einen zweiten Ausgangslogikblock mit einem Eingang, der mit dem Array bzw. dem Feld (12) verbunden ist, einen Eingang, der mit einem zweiten Bauelement-Eingangs-/Ausgangsstift (60) verbunden ist, einen Ausgang, der mit dem zweiten Bauelement-Eingangs-/Ausgangsstift (60) verbunden ist, und einen Ausgang, der mit einem Eingang der Auswahleinrichtung (82) verbunden ist.

4. Bauelement nach Anspruch 1, bei welchem der Multiplexer-Schaltungskomplex (132) des Ausgangslogikblocks einen Eingang aufweist, der mit einem Bauelement-Eingangs/Ausgangsstift (62) verbunden ist, und der Logikschaltungskomplex eine kombinatorische Logikschaltung (124) und ein getaktetes Logikbauelement (128) aufweist.

5. Bauelement nach Anspruch 1 oder 4, bei welchem der Multiplexer-Schaltungskomplex (132) ebenso einen Eingang aufweist, der mit einem zweiten Bauelement-Eingangs-/Ausgangsstift durch einen zweiten Ausgangslogikblock verbunden ist.

6. Programmierbares Logikbauelement nach Anspruch 1, das weiter folgendes aufweist:

eine Anzahl von anwendungsspezifischen bzw. zweckgebundenen Bauelement-Eingangsstiften (14, 16, 18, 20), die mit dem Array bzw. der Anordnung durch Zeilenpuffer (22, 24, 26, 28) verbunden sind;
eine Anzahl von Ausgangslogikblöcken (48, 50, 52, 54) mit Eingängen, die mit dem Array bzw. dem Feld (12) verbunden sind, und mit Eingängen und Ausgängen, die mit den Bauelement-Eingangs-/Ausgangsstiften (60, 62, 64, 66) verbunden sind, die damit korrespondieren;
wobei der Multiplexer-Schaltungskomplex von wenigstens einem Ausgangslogikblock (48, 50, 52, 54) dazu dient, der Auswahleinrichtung (82, 104) ein Signal zu liefern, das aus dem folgenden ausgewählt wird: ein Ausgang von einer kombinatorischen Logikschaltung (124) innerhalb des Ausgangslogikblockes, einem Ausgang von einem getakteten Bauelement (128) innerhalb des Ausgangslogikblockes und einem Signal, das auf dem entsprechenden Bauelement-Eingangs-/Ausgangsstift (62) anliegt bzw. vorhanden ist.

7. Bauelement nach Anspruch 6, bei welchem der Multiplexer-Schaltungskomplex (132) das Signal mit der möglichen Auswahl eines Signals liefert, das auf einem Bauelement-Eingangs-/Ausgangsstift (60, 62) anliegt, der einem Ausgangslogikblock entspricht, der nicht direkt mit der Auswahleinrichtung verbunden ist.

Revendications

1. Dispositif logique programmable comprenant une matrice de portes ET-OU (12), une mémoire-tampon de commande de ligne (86, 106) ayant une sortie reliée à la matrice, et un bloc logique de sortie (48, 50, 52, 54) comprenant un ensemble de circuits de multiplexage (132) et un ensemble de circuits logiques (124, 128) reliés à des entrées de l'ensemble de circuits de multiplexage (132), ledit dispositif logique programmable comprenant en outre une broche d'entrée (78, 100), un sélecteur (82, 104) dont la sortie est reliée à la mémoire-tampon de commande de ligne (86, 106), une première entrée reliée à la broche d'entrée (78, 100) et une deuxième entrée reliée à une sortie de l'ensemble de circuits de multiplexage (132), le sélecteur (82, 104) comprenant en outre un verrou de programme (122) pour mémoriser des informations du programme déterminant quelle entrée du sélecteur est reliée à la sortie du sélecteur, et dans lequel la broche d'entrée (78, 100) est en outre reliée à un ensemble de circuits tampons (108, 84), pour qu'ainsi ledit sélecteur (82, 104) fournisse des données venant de ladite première ou de ladite deuxième entrée à ladite mémoire-tampon de commande de ligne (86,

106) en fonction desdites informations du programme, et pour qu'ainsi lesdites informations du programme amènent ledit sélecteur à ignorer le signal présent sur ladite première entrée lorsque ladite broche d'entrée (78, 100) fournit des signaux de commande.

2. Dispositif selon la revendication 1, dans lequel le bloc logique de sortie (50) a une entrée reliée à la matrice, une entrée reliée à une broche d'entrée/sortie (62) du dispositif et une sortie reliée à la broche d'entrée/sortie (62) du dispositif.

3. Dispositif selon la revendication 2, comprenant en outre un deuxième bloc logique de sortie (48) ayant une entrée reliée à la matrice (12), une entrée reliée à une deuxième broche d'entrée/sortie (60) du dispositif, une sortie reliée à la deuxième broche d'entrée/sortie (60) du dispositif et une sortie reliée à une entrée dudit sélecteur (82).

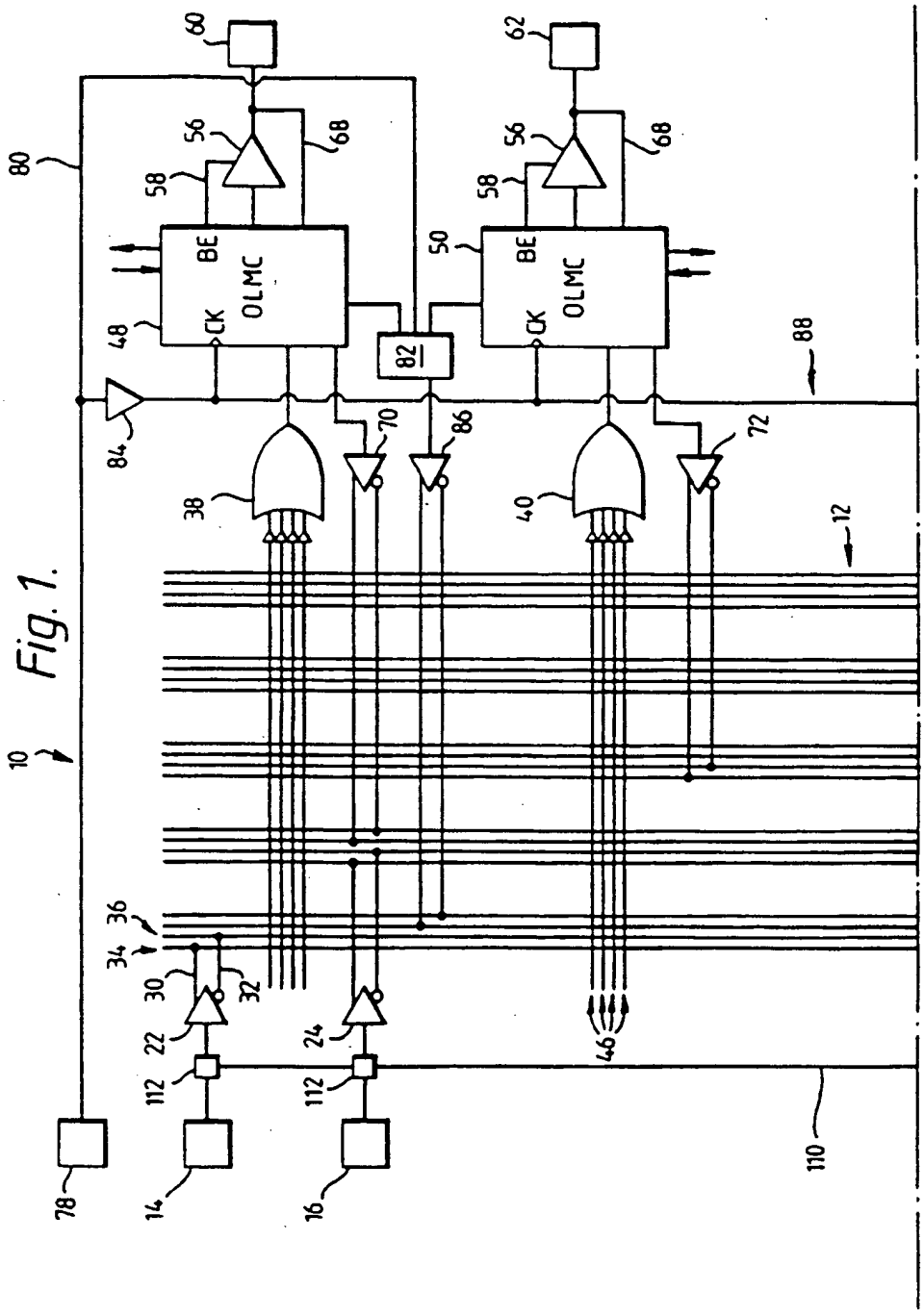
4. Dispositif selon la revendication 1, dans lequel l'ensemble de circuits de multiplexage (132) du bloc logique de sortie a une entrée reliée à une broche d'entrée/sortie (62) du dispositif, et dans lequel ledit ensemble de circuits logiques comprend un circuit logique combinatoire (124) et un circuit logique cadencé (128).

5. Dispositif selon la revendication 1 ou 4, dans lequel ledit ensemble de circuits de multiplexage (132) a également une entrée reliée à une deuxième broche d'entrée/sortie du dispositif, par l'intermédiaire d'un deuxième bloc logique de sortie.

6. Dispositif logique programmable selon la revendication 1, et comprenant en outre :

une pluralité de broches spécialisées d'entrée (14, 16, 18, 20) du dispositif, reliées à ladite matrice par l'intermédiaire de mémoires-tampons de lignes (22, 24, 26, 28) ;
une pluralité de blocs logiques de sortie (48, 50, 52, 54) ayant des entrées reliées à ladite matrice (12), et ayant des entrées et des sorties reliées à des broches d'entrée/sortie (60, 62, 64, 55) du dispositif, qui leur correspondent ;
dans lequel l'ensemble de circuits de multiplexage d'au moins un bloc logique de sortie (48, 50, 52, 54) sert à fournir audit sélecteur (82, 104) un signal choisi parmi les signaux suivants : une sortie venant d'un circuit logique combinatoire (124) situé dans le bloc logique de sortie, une sortie venant d'un dispositif cadencé (128) situé dans le bloc logique de sortie, et un signal présent sur la broche d'entrée/sortie (62) correspondante.

7. Dispositif selon la revendication 6, dans lequel ledit ensemble de circuits de multiplexage (132) fournit le signal, avec en outre une sélection possible d'un signal présent sur une broche d'entrée/sortie (60, 62) du dispositif, correspondant à un bloc logique de sortie non directement relié audit sélecteur.


60
62
56
68
58
80
BE
OLMC
CK
48
50
82
88
84
70
86
72
38
40
12
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36
34
30
32
22
24
46
112
112
78
14
16
110

Fig. 1.

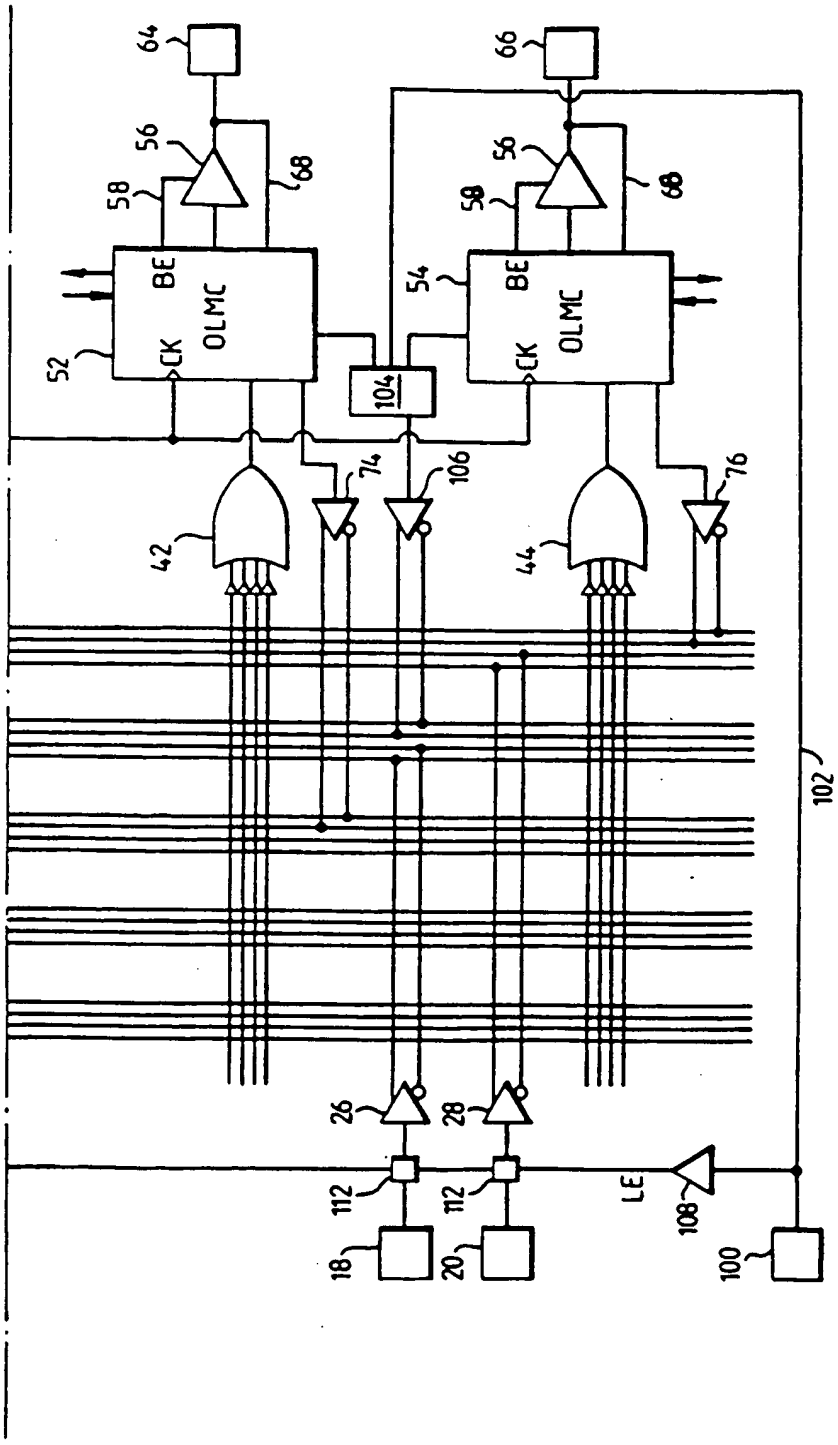
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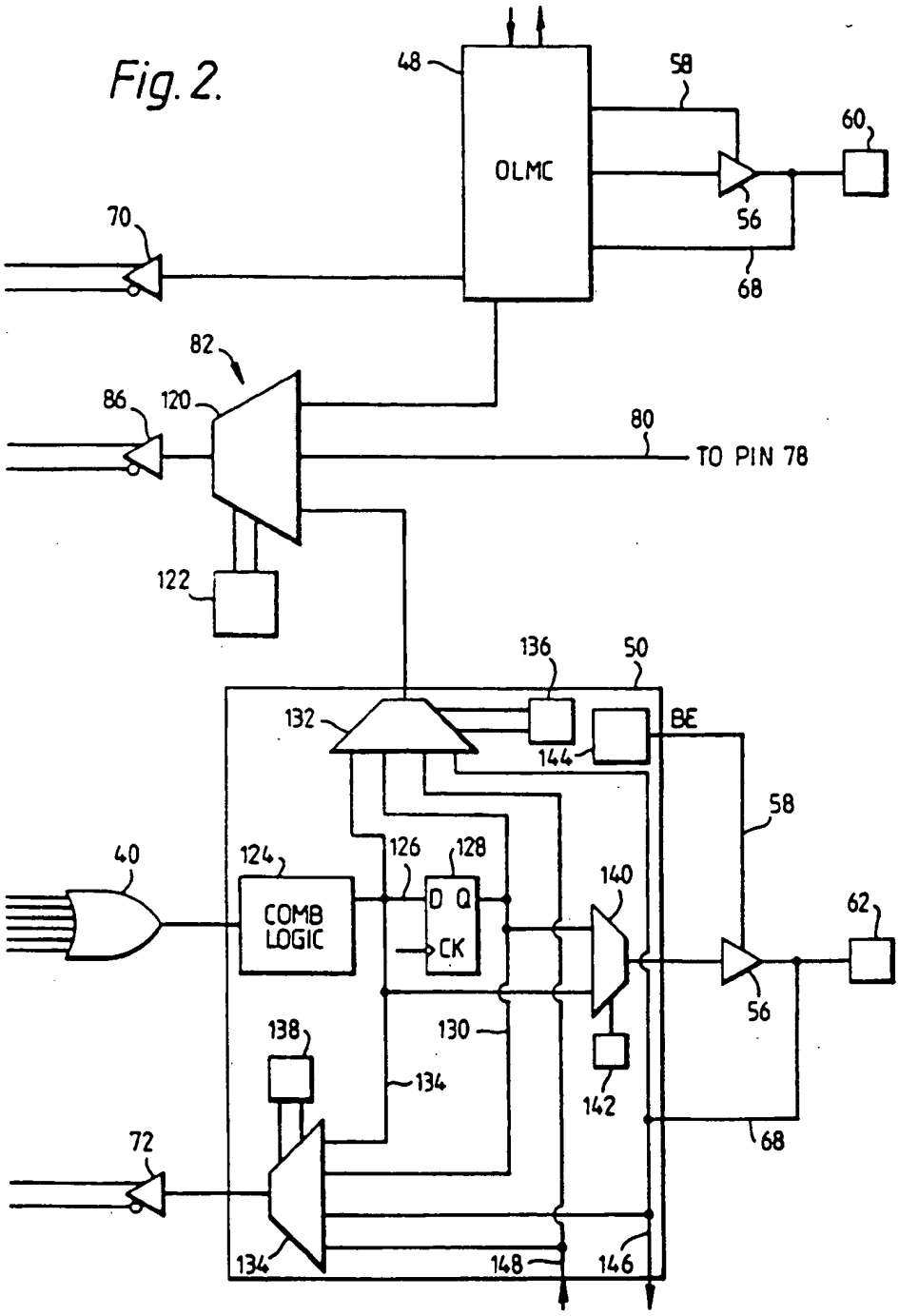
Fig. 1(cont.)

Fig. 2.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